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(54) Title: NON–OXYGEN PRECIPITATING CZOCHRALSKI SILICON WAFERS

(57) Abstract

The present invention relates to a process for the treatment of Czochralski single crystal silicon wafers to dissolve existing oxygen clusters and precipitates, while preventing their formation upon a subsequent oxygen precipitation heat treatment. The process comprises (i) heat–treating the wafer in a rapid thermal annealer at a temperature of at least 1150°C in an atmosphere having an oxygen concentration of at least 1000 ppma, or alternatively (ii) heat–treating the wafer in a rapid thermal annealer at a temperature of at least about 1150°C and then controlling the rate of cooling from the maximum temperature achieved during the heat–treatment through a temperature range in which vacancies are relatively mobile in order to reduce the number density of vacancies in the single crystal silicon to a value such that oxygen precipitates will not form if the wafer is subsequently subjected to an oxygen precipitation heat–treatment.

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NON-OXYGEN PRECIPITATING CZOCHRALSKI SILICON WAFERS

BACKGROUND OF THE INVENTION

The present invention generally relates to the preparation of semiconductor material substrates, especially silicon wafers, which are used in the manufacture of electronic components. More particularly, the present invention relates to a process for the treatment of Czochralski single crystal silicon wafers to dissolve existing oxygen clusters and precipitates, while preventing their formation upon a subsequent oxygen precipitation heat treatment.

Single crystal silicon, which is the starting material for most processes for the fabrication of semiconductor electronic components, is commonly prepared with the so-called Czochralski process wherein a single seed crystal is immersed into molten silicon and then grown by slow extraction. As molten silicon is contained in a quartz crucible, it is contaminated with various impurities, among which is mainly oxygen. At the temperature of the silicon molten mass, oxygen comes into the crystal lattice until it reaches a concentration determined by the solubility of oxygen in silicon at the temperature of the molten mass and by the actual segregation coefficient of oxygen in solidified silicon. Such concentrations are greater than the solubility of oxygen in solid silicon at the temperatures typical for the processes for the fabrication of electronic devices. As the crystal grows from the molten mass and cools, therefore, the solubility of oxygen in it decreases rapidly, whereby in the resulting slices or wafers oxygen is present in supersaturated concentrations.

During the thermal treatment cycles typically employed in the fabrication of electronic devices, oxygen precipitate nucleation centers may form and ultimately grown into large oxygen clusters or precipitates. The presence of such precipitates in the active device region of the wafer can impair the operation of the device. Historically, to address this problem electronic device fabrication processes included a series of steps which were designed to produce silicon having a zone or region near

the surface of the wafer which is free of oxygen precipitates (commonly referred to as a "denuded zone" or a "precipitate free zone"). Denuded zones can be formed, for example, in a high-low-high thermal sequence such as (a) oxygen out-diffusion heat treatment at a high temperature (>1100 °C) in an inert ambient for a period of at least about 4 hours, (b) oxygen precipitate nuclei formation at a low temperature (600-750 °C), and (c) growth of oxygen (SiO_2) precipitates at a high temperature (1000-1150 °C). See, e.g., F. Shimura, Semiconductor Silicon Crystal Technology, Academic Press, Inc., San Diego California (1989) at pages 361-367 and the references cited therein.

More recently, however, advanced electronic device manufacturing processes such as DRAM manufacturing processes have begun to minimize the use of high temperature process steps. Although some of these processes retain enough of the high temperature process steps to produce a denuded zone, the tolerances on the material are too tight to render it a commercially viable product. Other current, highly advanced electronic device manufacturing processes contain no out-diffusion steps at all. Because of the problems associated with oxygen precipitates in the active device region, therefore, these electronic device fabricators must use silicon wafers which are incapable of forming oxygen precipitates anywhere in the wafer under their process conditions.

Accordingly, a process is needed by which existing oxygen clusters or precipitates in the silicon wafer may be dissolved, prior to the device fabrication, in such a way that future formation of oxygen precipitates within the wafer is prevented.

SUMMARY OF THE INVENTION

Among the objects of the invention, therefore, is the provision of a Czochralski single crystal silicon wafer, as well as the process for the preparation thereof, in which oxygen clusters and precipitates have been dissolved; and, the

provision of such a wafer which will not form oxygen precipitates or clusters upon being subjected to an oxygen precipitation heat treatment.

Briefly, therefore, the present invention is directed to a process for heat-treating a Czochralski single crystal silicon wafer in a rapid thermal annealer to dissolve oxygen clusters, and to prevent future precipitate formation resulting from a subsequent thermal processing step. The process comprises heat-treating the wafer at a temperature of at least about 1150 °C in an atmosphere having an oxygen concentration of at least about 1000 ppma to dissolve existing oxygen clusters and yield a wafer which is incapable of forming oxygen precipitates upon being subjected to an oxygen precipitation heat treatment.

The present invention is further directed to a process for heat-treating a Czochralski single crystal silicon wafer to dissolve oxygen precipitates or clusters, and to prevent future precipitate formation resulting from a subsequent thermal processing step. The process comprises heat-treating the wafer in a rapid thermal annealer at a temperature of at least about 1150 °C to dissolve existing oxygen clusters or precipitates, and controlling the cooling rate of the heat-treated wafer down to a temperature of less than about 950 °C to produce a wafer which is incapable of forming oxygen precipitates upon being subjected to an oxygen precipitation heat treatment.

The present invention is still further directed to a process for heat-treating a Czochralski single crystal silicon wafer to dissolve oxygen precipitates or clusters, and to prevent future precipitate formation resulting from a subsequent thermal processing step. The process comprises heat-treating the wafer in a rapid thermal annealer at a temperature of at least about 1150 °C in an atmosphere to dissolve existing oxygen clusters or precipitates. The heat-treated wafer is then cooled to a temperature between about 950 and 1150 °C at a rate in excess of about 20 °C, and then thermally annealed at a temperature between about 950 and 1150 °C to produce a wafer which is incapable of forming oxygen precipitates upon being subjected to an oxygen precipitation heat treatment.

Other objects and features of this invention will be in part apparent and in part pointed out hereinafter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention affords the means by which to obtain a single crystal silicon wafer having a reduced concentration of oxygen precipitates or clusters, as well as other defects to which these precipitates are related. Additionally, the present process yields a wafer which, during essentially any subsequent oxygen precipitation heat treatment (e.g., annealing the wafer at a temperature of 800 °C for four hours and then at a temperature of 1000 °C for sixteen hours), will not form oxygen precipitates. The process of the present invention therefore acts to annihilate or dissolve a variety of pre-existing defects such as large oxygen clusters and certain kinds of oxygen induced stacking fault ("OISF") nuclei throughout the wafer. The dissolved oxygen which remains in the wafer will not precipitate, even if the wafer is subjected to an oxygen precipitation heat treatment.

The starting material for the process of the present invention is a single crystal silicon wafer which has been sliced from a single crystal ingot grown in accordance with conventional Czochralski crystal growing methods. Such methods, as well as standard silicon slicing, lapping, etching, and polishing techniques are disclosed, for example, in F. Shimura, Semiconductor Silicon Crystal Technology, Academic Press, 1989, and Silicon Chemical Etching, (J. Grabmaier ed.) Springer-Verlag, New York, 1982 (incorporated herein by reference). The silicon wafer may be polished or, alternatively, it may be lapped and etched but not polished. In addition, the wafer may have vacancy or self-interstitial point defects as the predominant intrinsic point defect. For example, the wafer may be vacancy dominated from center to edge, self-interstitial dominated from center to edge, or it may contain a central core of vacancy of dominated material surrounded by an axially symmetric ring of self-interstitial dominated material.

Czochralski-grown silicon typically has an oxygen concentration within the range of about 5 x 10^{17} to about 9 x 10^{17} atoms/cm^3 (ASTM standard F-121-83). Because the oxygen precipitation behavior of the wafer is essentially erased by the present process (i.e., the wafer is essentially rendered non-oxygen precipitating, even if subjected to an oxygen precipitation heat treatment), the starting wafer may have an oxygen concentration falling anywhere within or even outside the range attainable by the Czochralski process. Depending upon the cooling rate of the single crystal silicon ingot from the temperature of the melting point of silicon (about 1410 °C) through the range of about 750 °C to about 350 °C, oxygen precipitate nucleation centers may form in the single crystal silicon ingot from which the wafer is sliced.

The presence or absence of these nucleation centers in the starting material is not critical to the present invention. Preferably, however, these centers are capable of being dissolved by the rapid thermal anneal heat-treatment of the present invention.

In accordance with the process of the present invention, a single crystal silicon wafer is first subjected a heat treatment step in which the wafer is heated to an elevated temperature. Preferably, this heat treatment step is carried out in a rapid thermal annealer in which the wafer is rapidly heated to a target temperature and annealed at that temperature for a relatively short period of time. In general, the wafer is subjected to a temperature in excess of 1150 °C, preferably at least 1175 °C, more preferably at least about 1200 °C, and most preferably between about 1200 °C and 1275 °C. The wafer will generally be maintained at this temperature for at least one second, typically for at least several seconds (e.g., at least 3), preferably for several tens of seconds (e.g., 20, 30, 40, or 50 seconds) and, depending upon the pre-existing defects, for a period which may range up to about 60 seconds (which is near the limit for commercially available rapid thermal annealers).

The rapid thermal anneal may be carried out in any of a number of commercially available rapid thermal annealing ("RTA") furnaces in which wafers are individually heated by banks of high power lamps. RTA furnaces are capable of rapidly heating a silicon wafer, e.g., they are capable of heating a wafer from room

temperature to 1200 °C in a few seconds. One such commercially available RTA furnace is the model 610 furnace available from AG Associates (Mountain View, CA).

Heat-treating the wafer at a temperature in excess of 1150 °C will cause the dissolution of a variety of pre-existing oxygen clusters and OISF nuclei. In addition, it will increase the number density of crystal lattice vacancies in the wafer.

Information obtained to date suggests that certain oxygen-related defects, such as ring oxidation induced stacking faults (OISF), are high temperature nucleated oxygen agglomerates catalyzed by the presence of a high concentration of vacancies. Furthermore, in high vacancy regions, oxygen clustering is believed to occur rapidly at elevated temperatures, as opposed to regions of low vacancy concentration where behavior is more similar to regions in which oxygen precipitate nucleation centers are lacking. Because oxygen precipitation behavior is influenced by vacancy concentration, therefore, the number of density of vacancies in the heat-treated wafer is controlled in the process of the present invention to avoid oxygen precipitation in a subsequent oxygen precipitation heat treatment.

In a first embodiment of the process of the present invention, the vacancy concentration in the heat-treated wafers is controlled, at least in part, by controlling the atmosphere in which the heat-treatment is carried out. Experimental evidence obtained to date suggests that the presence of a significant amount of oxygen suppresses the vacancy concentration in the heat-treated wafer. Without being held to any particular theory, it is believed that the rapid thermal annealing treatment in the presence of oxygen results in the oxidation of the silicon surface and, as a result, acts to create an inward flux of silicon self-interstitials. This inward flux of self-interstitials has the effect of gradually altering the vacancy concentration profile by causing recombinations to occur, beginning at the surface and then moving inward.

Regardless of the mechanism, the rapid thermal annealing step is carried out in the presence of an oxygen-containing atmosphere in the first embodiment of the process of the present invention; that is, the anneal is carried out in an atmosphere

containing oxygen gas (O_2), water vapor, or an oxygen-containing compound gas which is capable of oxidizing an exposed silicon surface. The atmosphere may thus consist entirely of oxygen or oxygen compound gas, or it may additionally comprise a non-oxidizing gas such as argon. It is to be noted, however, that when the atmosphere is not entirely oxygen, preferably the atmosphere will contain a partial pressure of oxygen of at least about 0.001 atmospheres (atm.), or 1,000 parts per million atomic (ppma). More preferably, the partial pressure of oxygen in the atmosphere will be at least about 0.002 atm. (2,000 ppma), still more preferably 0.005 atm. (5,000 ppma), and still more preferably 0.01 atm. (10,000 ppma).

Intrinsic point defects (vacancies and silicon self-interstitials) are capable of diffusing through single crystal silicon with the rate of diffusion being temperature dependant. The concentration profile of intrinsic point defects, therefore, is a function of the diffusivity of the intrinsic point defects and the recombination rate as a function of temperature. For example, the intrinsic point defects are relatively mobile at temperatures in the vicinity of the temperature at which the wafer is annealed in the rapid thermal annealing step, whereas they are essentially immobile for any commercially practical time period at temperatures of as much as 700 °C. Experimental evidence obtained to-date suggests that the effective diffusion rate of vacancies slows considerably at temperatures less than about 700 °C and perhaps as great as 800 °C, 900 °C, or even 1,000 °C, the vacancies can be considered to be immobile for any commercially practical time period.

In a second embodiment of the present invention, therefore, the concentration of vacancies in the heat-treated wafer is controlled, at least in part, by controlling the cooling rate of the wafer through the temperature range at which vacancies are relatively mobile. As the temperature of the wafer is decreased through this range of temperatures, the vacancies diffuse to the wafer surface and are annihilated, thus leading to a change in the vacancy concentration profile with the extent of change depending upon the length of time the wafer is maintained at a temperature within this range and the magnitude of the temperature; in general, greater temperatures and

longer diffusion times lead to increased diffusion. In general, the average cooling rate from the annealing temperature to the temperature at which vacancies are practically immobile (e.g., about 950 °C) is preferably no more than 20 °C per second, more preferably no more than about 10 °C, and still more preferably no more than about 5 °C per second.

Alternatively, the temperature of the wafer following the high temperature anneal may be reduced quickly (e.g., at a rate greater than about 20 °C/second) to a temperature of less than about 1150 °C but greater than about 950 °C and held for a time which is dependent upon the holding temperature. For example, for temperatures near 1150 °C, several seconds (e.g., at least about 2, 3, 4, 6 or more) may be sufficient whereas at temperatures near 950 °C several minutes (e.g., at least about 2, 3, 4, 6 or more) may be required to sufficiently reduce the vacancy concentration.

Once the wafer is cooled to a temperature outside the range of temperatures at which crystal lattice vacancies are relatively mobile in the single crystal silicon, the cooling rate does not appear to significantly influence the precipitating characteristics of the wafer and thus, does not appear to be narrowly critical.

Conveniently, the cooling step may be carried out in the same atmosphere in which the heating step is carried out. Suitable atmospheres include, for example, nitriding atmospheres (that is, atmospheres containing nitrogen gas (N_2) or a nitrogen-containing compound gas, such as ammonia, which is capable of nitriding an exposed silicon surface); oxidizing (oxygen-containing) atmospheres; non-oxidizing, non-nitriding atmospheres (such as argon, helium, neon, carbon dioxide), and combinations thereof.

While the rapid thermal treatments employed in this process may result in the out-diffusion of a small amount of oxygen from the surface of the front and back surfaces of the wafer, the resulting heat-treated wafer has a substantially uniform interstitial oxygen concentration as a function of distance from the silicon surface. For example, a heat-treated wafer will have a substantially uniform concentration of

interstitial oxygen from the center of the wafer to regions of the wafer which are within about 15 microns of the silicon surface, more preferably from the center of the silicon to regions of the wafer which are within about 10 microns of the silicon surface, even more preferably from the center of the silicon to regions of the wafer which are within about 5 microns of the silicon surface, and most preferably from the center of the silicon to regions of the wafer which are within about 3 microns of the silicon surface. In this context, a substantially uniform oxygen concentration shall mean a variance in the oxygen concentration of no more than about 50%, preferably no more than about 20%, and most preferably no more than about 10%.

In view of the above, it will be seen that the several objects of the invention are achieved. As various changes could be made in the above compositions and processes without departing from the scope of the invention, it is intended that all matter contained in the above description be interpreted as illustrative and not in a limiting sense.

We claim:

1. A process for heat-treating a Czochralski single crystal silicon wafer to dissolve oxygen precipitates, the process comprising heat-treating the wafer in a rapid thermal annealer at a temperature of at least about 1150 °C in an atmosphere having an oxygen concentration of at least about 1000 ppma.

2. The process of claim 1 wherein the wafer is heat-treated at a temperature between about 1200 °C to about 1275 °C.

3. The process of claim 1 or 2 wherein the atmosphere has an oxygen concentration of at least about 2000 ppma.

4. The process of claim 1 or 2 wherein the atmosphere has an oxygen concentration of at least about 5000 ppma.

5. The process of claim 1 or 2 wherein the atmosphere has an oxygen concentration of at least about 10,000 ppma.

6. The process of claim 1 or 2 wherein the wafer is heat-treated for at least about 20 seconds.

7. The process of claim 1 or 2 wherein the wafer is heat-treated for at least about 40 seconds.

8. A process for heat-treating a Czochralski single crystal silicon wafer to dissolve oxygen precipitates, the process comprising heat-treating the wafer in a rapid thermal annealer at a temperature of at least about 1150 °C and controlling the rate of cooling from the maximum temperature achieved during the heat-treatment through a

temperature range in which vacancies are relatively mobile to reduce the number density of vacancies in the single crystal silicon to a value such that oxygen precipitates will not form in the heat-treated wafer upon subjecting the wafer to an oxygen precipitation heat-treatment.

9. The process of claim 8 wherein the wafer is heat-treated at a temperature between about 1200 °C to about 1275 °C.

10. The process of claim 8 wherein the cooling rate is controlled between the maximum temperature achieved during the heat-treatment to a temperature of about 900 °C.

11. The process of claim 8, 9 or 10 wherein the cooling rate is less than about 20°C/second.

12. The process of claim 8, 9 or 10 wherein the cooling rate is less than about 10°C/second.

13. The process of claim 8, 9 or 10 wherein the cooling rate is less than about 5°C/second.

14. The process of claim 8, 9 or 10 wherein the wafer is cooled in a nitriding atmosphere.

15. The process of claim 8, 9 or 10 wherein the wafer is cooled in an oxidizing atmosphere.

16. The process of claim 8, 9 or 10 wherein the wafer is cooled in a non-nitriding, non-oxidizing atmosphere.

17. A process for heat-treating a Czochralski single crystal silicon wafer to dissolve oxygen clusters and to prevent future precipitate formation resulting from an oxygen precipitation heat treatment, the process comprising:

heat-treating the wafer at a temperature of at least about 1150 °C in a rapid thermal annealer to dissolve pre-existing oxygen clusters;

cooling the heat-treated wafer to a temperature between about 950 and 1150 °C at a rate in excess of about 20 °C;

thermally annealing the cooled wafer at a temperature between about 950 and 1150 °C to produce a wafer which is incapable of forming oxygen precipitates upon being subjected to an oxygen precipitation heat treatment.

18. The process of claim 17 wherein the wafer is heat-treated at a temperature between about 1200 and about 1275 °C.

19. The process of claim 17 or 18 wherein the cooled wafer is thermally annealed at a temperature of about 950 °C for about 2 minutes.

20. The process of claim 17 or 18 wherein the cooled wafer is thermally annealed at a temperature of about 950 °C for about 6 minutes.

21. The process of claim 17 or 18 wherein the cooled wafer is thermally annealed at a temperature of about 1150 °C for about 2 seconds.

22. The process of claim 17 or 18 wherein the cooled wafer is thermally annealed at a temperature of about 1150 °C for about 6 seconds.

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The present invention relates to a process for the treatment of Czochralski single crystal silicon wafers to dissolve existing oxygen clusters and precipitates, while preventing their formation upon a subsequent oxygen precipitation heat treatment. The process comprises (i) heat–treating the wafer in a rapid thermal annealer at a temperature of at least 1150°C in an atmosphere having an oxygen concentration of at least 1000 ppma, or alternatively (ii) heat–treating the wafer in a rapid thermal annealer at a temperature of at least about 1150°C and then controlling the rate of cooling from the maximum temperature achieved during the heat–treatment through a temperature range in which vacancies are relatively mobile in order to reduce the number density of vacancies in the single crystal silicon to a value such that oxygen precipitates will not form if the wafer is subsequently subjected to an oxygen precipitation heat–treatment.

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INTERNATIONAL SEARCH REPORT

In. .tional Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/322

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JACOB M ET AL: "Influence of RTP on vacancy concentrations" SEMICONDUCTOR PROCESS AND DEVICE PERFORMANCE MODELLING. SYMPOSIUM, SEMICONDUCTOR PROCESS AND DEVICE PERFORMANCE MODELLING. SYMPOSIUM, BOSTON, MA, USA, 2-3 DEC. 1997, pages 129-134, XP000856047 1998, Warrendale, PA, USA, Mater. Res. Soc, USA ISBN: 1-55899-395-9 page 130 -page 131 --- -/--	1-7

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22 May 2000	02. 06. 2000
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Authorized officer Gélébart, J

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropnate, of the relevant passages	Relevant to claim No.
A	HAWKINS G A ET AL: "Effect on rapid thermal processing on oxygen precipitation in silicon" DEFECTS IN ELECTRONIC MATERIALS. SYMPOSIUM, BOSTON, MA, USA, 30 NOV.-3 DEC. 1987, pages 197-200, XP000856847 1988, Pittsburgh, PA, USA, Mater. Res. Soc, USA ISBN: 0-931837-72-3 page 199 ---	1
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